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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
9694D-000025/US

Application Number	Filed
10/551,266	**September 29, 2005**
First Named Inventor: **Toshiro AKINO**	
Art Unit: **2816**	Examiner: **Colleen J. O'Toole**

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a Notice of Appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

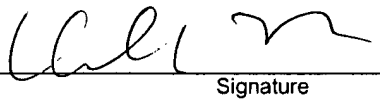
I am the

☐ applicant/inventor

☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

☒ attorney or agent of record.
Registration number 34,313.

☐ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 __



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April 9, 2008
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of __forms are submitted.

PATENT
9694D-000025/US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	Toshiro AKINO	Group:	2816
App. No.:	**10/551,266**	Conf.:	3385
Filed:	September 29, 2005	Examiner:	Colleen J. O'Toole

For: LATERAL BIPOLAR CMOS INTEGRATED CIRCUIT

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April 9, 2008

REASONS FOR PRE-APPEAL BRIEF REQUEST FOR REVIEW

Sir:

Concurrent to the filing of a Notice of Appeal and Request for Pre-Appeal Review, the following remarks are submitted in support of Appellant's Request for Pre-Appeal Brief Conference in connection with the above-identified application.[1] Claims 1-8 are pending. Of those, claim 1 is independent.

[1] Off. Gaz. Patent & Trademark Office, Vol. 1296, No. 2, July 12, 2005.

A Pre-Appeal Conference is requested to review the rejection of claims 1-4 under 35 U.S.C. §103(a) as being unpatentable over "On the Power Dissipation in Dynamic Threshold Silicon-on-Insulator CMOS Inverter," IEEE Transactions on Electron Devices, Vol. 45, No. 8, August 1998 ("*Jin*") in view of *Yamaguchi* U.S. Patent No. 5,557,231 ("*Yamaguchi*") and the rejections of claims 5-8 under 35 U.S.C. §103(a) as being unpatentable over *Jin* in view of *Yamaguchi*, and in further view of Japanese Patent Publication No. 10-189957 ("*Shimomura*") (as cited in the Information Disclosure Statement dated September 29, 2005).

Initially, please refer to Applicants' arguments contained in the February 11, 2008 Request for Reconsideration ("*Request for Reconsideration*").

Rejection of claims 1-4 under 35 U.S.C. §103(a) – *Jin & Yamaguchi*

Jin allegedly teaches a silicon-on-insular dynamic threshold voltage MOSFET (SOI DTMOS) in FIG. 3. An input 1 is said to be connected to stage n-1, which allegedly connects to an inverter containing a p-channel transistor and an n-channel transistor. An output 0 is allegedly connected to stage n, and FIG. 3 is said to further include a source Vdd and a source GND. (*Jin*, pages 1717-1718).

In the Final Office Action dated November 9, 2007 ("*Final Office Action*") the Examiner acknowledges that "*Jin* does not teach a first or second current source," and Applicants agree. (*Final Office Action*, page 3).

The Examiner attempts to cure this deficiency of *Jin* by citing FIG. 13 of *Yamaguchi*. (*Final Office Action*, pages 3-4). FIG. 13 of *Yamaguchi* allegedly teaches an example of the bias selecting circuit 32' shown in FIG. 9 which is said to provide the substrate bias to the functional circuit 110. Since the bias selecting circuit 32' of FIG. 13 is said to have portions in common with the bias selecting circuit 32 shown in FIG. 8 of *Yamaguchi*, a discussion of both follows below. (*Yamaguchi*, col. 12, lines 58-59).

FIG. 8 allegedly teaches that the bias selecting circuit 32 includes NMOS transistors 321 and 322. The NMOS transistor 321 allegedly has its source connected to receive the substrate

bias VBB1, its drain connected to the silicon substrate 1 together with the drain of the NMOS transistor 322, and its gate connected to receive the control signal /CNT. The NMOS transistor 322 is said to have its source connected to receive the substrate bias VBB2, and its gate connected to receive the signal CNT. Operationally, *Yamaguchi* allegedly teaches that in the standby state, the control signal /CNT is set to the high level, NMOS transistor 321 is turned on, and the substrate bias VBB1 is supplied to the silicon substrate 1, and in the active state, the control signal CNT is set to the high level, the NMOS transistor 322 is turned on, and the substrate bias VBB2 is supplied to the silicon substrate 1. According to *Yamaguchi*, this structure allows the substrate bias applied to the silicon substrate 1 to be changed. (*Yamaguchi*, col. 11, lines 16-33). [Applicants note that, in FIG. 1 *Yamaguchi* allegedly teaches that a semiconductor device 200, including a functional circuit 110, a first bias generating circuit 30, a second bias generating circuit 31, and a bias selecting circuit 32, is formed on a silicon substrate 1. (*Yamaguchi*, col. 8, lines 18-23).]

The bias selecting circuit 32' of FIG. 13 is said to differ from the bias selecting circuit 32 in FIG. 8 by having an NMOS transistor 323 responsive to the control signal /CNT for selecting the substrate bias VBB3 and an NMOS transistor 324 responsive to the control signal CNT for selecting the substrate bias VBB4. *Yamaguchi* allegedly teaches that other features of the bias selecting circuit 32' are the same as the bias selecting circuit 32 shown in FIG. 8. (*Yamaguchi*, col. 11, lines 39-49, and col. 12, lines 51-59).

Applicants respectfully disagree with the Examiner's assertion that *Yamaguchi* cures the deficiencies of *Jin*, and specifically with the Examiner's allegation that "*Yamaguchi* teaches a current source (321) in Figure 13 connected with the p-type base terminal of the n-channel MOS (the NMOS of the inverter) and a current source (323) connected with the n-type base terminal of the p-channel MOS transistor (the PMOS of the inverter)." (*Final Office Action*, page 3).

Applicants respectfully submit that, because the NMOS transistors 321 and 323 merely supply substrate bias VBB2 and VBB3 according to control signals CNT and /CNT, respectively, these transistors are used solely to bias the silicon substrate and cannot be considered current

sources. In fact, *Yamaguchi* explicitly states in reference to FIG. 8 that "by this simple structure, the substrate bias applied to the silicon substrate 1 can be changed." (*Yamaguchi*, col. 11, lines 32-33). Therefore, Applicants submit that nothing in *Yamaguchi* teaches or suggests "a current source connected with the p-type base terminal of the n-channel MOS transistor" and "a current source connected with the n-type base terminal of the p-channel MOS transistor" as recited by claim 1.

In the Advisory Action dated March 3, 2008 ("*Advisory Action*"), the Examiner argues that "Transistors 321 and 323 inherently generate current when activated by the control signals CNT and /CNT. Therefore, NMOS transistors 321 and 323 fulfill the current source limitations recited in claim 1." (*Advisory Action*, page 2).

Again, Applicants respectfully disagree with the Examiner. *Yamaguchi* in FIG. 13 allegedly teaches that the substrate of an NMOS transistor is connected with NMOS transistors 321 and 322, and that the NMOS transistors 321 and 322 supply a substrate bias VBB1 of -3 V and VBB2 of 0 V according to control signal /CNT and control signal CNT, respectively. Thus, the bias supplied to the substrate of the NMOS transistor is between -3 V and 0 V.

As further illustrated in FIG. 13 of *Yamaguchi*, the source of the NMOS transistor is connected with a level of 0 V, and therefore no current is flown between the substrate and the source of the NMOS transistor. Accordingly, Applicants submit that the bias selection circuit 32' cannot function as "a current source" as recited by claim 1.

For at least these reasons, Applicants respectfully request that the rejection of claim 1 be withdrawn, and that the rejections of claims 2-4 also be withdrawn, at least by virtue of their dependency upon claim 1.

Rejection of claims 5-8 under 35 U.S.C. §103(a) – *Jin & Yamaguchi & Shimomura*

Applicants submit that, even if *Shimomura* could be combined with *Jin* and *Yamaguchi* (which Applicants do not admit), nothing in *Shimomura* cures the deficiencies of *Jin* and *Yamaguchi* discussed above with respect to claim 1. Therefore, Applicants respectfully request that the rejections of claims 5-8 be withdrawn, at least by virtue of their dependency upon claim 1.

CONCLUSION

In view of the above remarks, Appellants request the Pre-Appeal Brief Conference to find in favor of Appellants' positions and arrange for withdrawal of the above-noted rejections, culminating in the sending of a Notice of Allowance of the pending claims.

Should there be any outstanding matters that need to be resolved in the present application, the Pre-Appeal Brief Review Board is respectfully requested to contact the undersigned at the telephone number below. If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

By _____

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